**Assignment 7**

**Assignment** All assignments are to be submitted strictly before start of next lab session through online only. Late assignments will not be entertained and will be awarded ‘0’ marks.

1. **Verilog code and testbench for T Flip-Flop for positive edge triggered.**

**Ans: Link1:** [**https://www.edaplayground.com/x/qhrm**](https://www.edaplayground.com/x/qhrm)

**2. Identify the logic from the Verilog code below. (hint: Create testbench to identify).**

module circuit\_1 (input A, B, output C);

assign C = A ? B : C;

// ? : is the conditional operator (e.g. w=x ? y : z ; if x=true, then w=y if x =false then w=z)

endmodule

**Ans: Link2:** [**https://www.edaplayground.com/x/9uAy**](https://www.edaplayground.com/x/9uAy)

**3. Identify the logic from the Verilog code below.** (hint: Create testbench to identify).

module circuit\_1 (input A, B, output C);

assign C = A ? B : C;

// ? : is the conditional operator (e.g. w=x ? y : z ; if x=true, then w=y if x =false then w=z)

endmodule

**Ans: Link3:** [**https://www.edaplayground.com/x/9uAy**](https://www.edaplayground.com/x/9uAy)

**Self-Practice and self-evaluation**

1. Verilog code and testbench for D Flip-Flop for negative edge triggered.

2. Identify the logic for the code below by writing the testbench

module circuit\_2 (input D\_in, en, rst, output q);

assign q = !(rst ==1’b0) ? 0 : en ? D\_in : q;

endmodule

3. Identify the logic for the code below by writing the testbench

module circuit\_2 (output reg q, input d, en);

always @ (en, d)

if (en ==1’b1) q &lt;= d;

endmodule

4. Identify the logic for the code below by writing the testbench

module circuit\_3 (q, q\_bar, d, set, rst, clk);

input d, set, rst, clk;

output reg q;

output q\_bar;

assign q\_bar = !q;

always @ (posedge clk) // code enters here only at rising edge or positive edge of clock

// this also makes set and reset signals synchronous to clock edge only

if (rst == 1’b0) q &lt;= 0; // operator ‘&lt;=’ is the non-blocking assignment operator

else if (set == 1’b0) q&lt;=1;

else q &lt;= d;

endmodule